IN THE CLAIMS:

All of the claims that remain pending and under consideration in the above-referenced application are reproduced below, in clean form, for the sake of clarity. In addition, a marked-up version of each amended claim is enclosed herewith to clearly identify each change that has been made thereto.

Please cancel claims 15, 36, 57, and 77 without prejudice or disclaimer.

Please enter the claims as follows:

1. (Twice amended) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over said active surface, said tape including at least one slot formed therethrough, each of said plurality of bond pads being exposed through said at least one slot, at least one end of said at least one slot extending beyond an outer periphery of said semiconductor die;

a substrate element positioned over said tape opposite said semiconductor die, said substrate element including a plurality of contact areas, each contact area of said plurality corresponding to a bond pad of said plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through said substrate element and aligned with said at least one slot of said tape, said substrate element further including a contact pad in communication with each contact area of said plurality of contact areas by way of a substantially laterally extending conductive trace;

a quantity of encapsulant material substantially filling a volume defined by said at least one slot of said tape and said at least one opening of said substrate element; and

a coverlay secured to a surface of said substrate element opposite said tape, said coverlay substantially covering at least said at least one opening through said substrate element.

2. (Previously amended) The semiconductor device package of claim 1, wherein said plurality of bond pads is arranged substantially linearly along a central region of said active surface of said semiconductor die.

3. The semiconductor device package of claim 1, wherein said tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of said semiconductor die.

4. The semiconductor device package of claim 3, wherein said substrate element has a coefficient of thermal expansion similar to said coefficient of thermal expansion of said material of said semiconductor die.

5. (Previously amended) The semiconductor device package of claim 1, wherein both ends of said at least one slot formed through said tape extend beyond said outer periphery of said semiconductor die.

6. The semiconductor device package of claim 1, wherein said tape is adhesively secured to said active surface of said semiconductor die and to said substrate element.

7. The semiconductor device package of claim 1, wherein said substrate element comprises at least one of an interposer and a carrier substrate.

8. The semiconductor device package of claim 1, wherein said substrate element comprises silicon.

9. The semiconductor device package of claim 1, wherein said quantity of encapsulant material substantially encapsulates each intermediate conductive element.

10. The semiconductor device package of claim 9, wherein said quantity of encapsulant material protrudes above a major plane of an exposed surface of said substrate element opposite said semiconductor die.

11. The semiconductor device package of claim 1, wherein said substrate element includes a recessed area adjacent said at least one opening, each contact area of said plurality of contact areas being located within said recessed area.

12. (Previously amended) The semiconductor device package of claim 11, wherein said quantity of encapsulant material substantially fills said recessed area.

13. The semiconductor device package of claim 12, wherein said quantity of encapsulant material substantially encapsulates each said intermediate conductive element.

14. The semiconductor device package of claim 12, wherein said quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of said substrate element.

16. (Amended) The semiconductor device package of claim 1, wherein said coverlay comprises a recessed area within which each intermediate conductive element is contained.

17. (Amended) The semiconductor device package of claim 1, wherein said coverlay is secured to said substrate element with an adhesive material.

18. The semiconductor device package of claim 17, wherein said adhesive material comprises a pressure sensitive adhesive material.

19. (Amended) The semiconductor device package of claim 1, wherein contact pads of said substrate element are exposed through or beyond said coverlay.

20. The semiconductor device package of claim 1, further comprising discrete conductive elements protruding from at least some of said contact pads.

21. (Amended) A semiconductor device assembly, comprising:

a semiconductor die with at least one bond pad on an active surface thereof;

a tape secured to said active surface, said tape including a slot formed therethrough with said at least one bond pad being exposed through said slot, at least one end of said slot extending beyond an outer periphery of said semiconductor die;

a substrate element positioned over said semiconductor die opposite said tape from said semiconductor die, said substrate element including at least one opening formed therethrough through which said at least one bond pad is exposed; and

a coverlay secured to a surface of said substrate element opposite said tape, said coverlay substantially covering at least said at least one opening through said substrate element.

22. The assembly of claim 21, wherein said semiconductor die includes a plurality of bond pads arranged substantially linearly along a central region of said active surface.

23. The assembly of claim 21, wherein said tape has a similar coefficient of thermal expansion to a coefficient of thermal expansion of said substrate element.

24. (Previously amended) The assembly of claim 23, wherein said semiconductor die has a similar coefficient of thermal expansion to said coefficient of thermal expansion of said substrate element.

25. The assembly of claim 21, wherein two ends of said slot extend beyond said outer periphery of said semiconductor die.

26. The assembly of claim 21, wherein said at least one end of said slot receives encapsulant material.

27. (Previously amended) The assembly of claim 25, wherein one of said two ends of said slot is positioned so as to facilitate displacement of air from said slot while an encapsulant

material is being introduced at least into a volume defined by said slot from the other of said two ends.

28. (Previously amended) The assembly of claim 21, wherein said substrate element comprises at least one of an interposer and a carrier substrate.

29. The assembly of claim 21, wherein said substrate element includes a recessed area formed adjacent said at least one opening in a surface of said substrate element located opposite said tape.

30. The assembly of claim 29, wherein said substrate element includes at least one contact area corresponding to said at least one bond pad of said semiconductor die.

31. The assembly of claim 30, wherein said at least one contact area is located within said recessed area.

32. The assembly of claim 31, wherein said recessed area receives a portion of an intermediate conductive element that extends between said at least one bond pad and said at least one contact area.

33. The assembly of claim 21, wherein said substrate element includes at least one contact area that corresponds to said at least one bond pad of said semiconductor die and at least one contact pad in electrical communication with said at least one contact area.

34. (Previously amended) The assembly of claim 33, further comprising at least one intermediate conductive element electrically connecting said at least one bond pad to said at least one contact area.

35. The assembly of claim 34, wherein said at least one intermediate conductive element extends through said slot of said tape and said at least one opening of said substrate element.

37. (Amended) The assembly of claim 21, wherein said coverlay includes a recessed area configured to communicate with said at least one opening.

38. The assembly of claim 37, wherein said recessed area is configured to receive a portion of at least one intermediate conductive element electrically connecting said at least one bond pad of said semiconductor die to a contact area on a surface of said substrate element adjacent said at least one opening formed therethrough.

39. (Amended) The assembly of claim 21, wherein said coverlay, said at least one opening formed through said substrate element, said slot formed through said tape, and said semiconductor die together form a receptacle.

40. The assembly of claim 39, wherein said receptacle at least partially contains a quantity of encapsulant material.

41. (Twice amended) A method for packaging at least an active surface of a semiconductor die, comprising:

positioning a tape over the active surface so that at least one bond pad on the active surface is exposed through a slot formed through said tape and at least one end of said slot extends beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape so that said at least one bond pad is exposed through at least one opening formed through said substrate element and aligned with said slot, said substrate element including at least one contact area corresponding to said at least one bond pad;

electrically connecting said at least one bond pad to said at least one contact area;

securing a coverlay to an exposed surface of said substrate element to substantially cover said at least one opening formed through said substrate element; and

introducing encapsulant material through said at least one end into a receptacle formed by said coverlay, said at least one opening, said slot, and said semiconductor die from a location opposite the semiconductor die from said tape.

42. The method of claim 41, wherein said positioning said tape comprises positioning over the semiconductor die a tape having a similar coefficient of thermal expansion to a coefficient of thermal expansion of the semiconductor die.

43. The method of claim 42, wherein said positioning said substrate element comprises positioning over said tape a substrate element having a similar coefficient of thermal expansion to said coefficient of thermal expansion of the semiconductor die.

44. The method of claim 43, wherein said positioning said substrate element comprises positioning a substrate element comprising silicon over said tape.

45. The method of claim 41, wherein said positioning said tape comprises orienting said slot with another end thereof extending laterally beyond said outer periphery of the semiconductor die.

46. The method of claim 41, further including securing said tape to the active surface of the semiconductor die.

47. The method of claim 46, wherein said securing comprises adhering said tape to the active surface.

48. The method of claim 41, wherein said positioning said substrate element comprises positioning at least one of an interposer and a carrier substrate over said tape.

49. The method of claim 41, wherein said positioning said substrate element comprises positioning over said tape a substrate element comprising a recessed area adjacent said at least one opening and including therein said at least one contact area.

50. (Previously amended) The method of claim 49, wherein said introducing comprises introducing a portion of said encapsulant material into said recessed area.

51. The method of claim 41, wherein said electrically connecting comprises connecting at least one intermediate conductive element between said at least one bond pad and said at least one contact area.

52. The method of claim 51, wherein said connecting said at least one intermediate conductive element comprises wire bonding.

53. The method of claim 51, wherein said connecting said at least one intermediate conductive element comprises extending said at least one intermediate conductive element through said slot formed through said tape and said at least one opening formed through said substrate element.

54. The method of claim 41, wherein said positioning said coverlay comprises positioning over said substrate element a coverlay including a recessed area alignable over said at least one opening and over intermediate conductive elements extending through said at least one opening.

55. The method of claim 41, further including securing said substrate element to said tape.

56. The method of claim 55, wherein said securing comprises adhesively securing said substrate element to said tape.

58. (Amended) The method of claim 41, wherein said securing comprises securing said coverlay to said substrate element with a pressure sensitive adhesive.

59. The method of claim 58, wherein said securing comprises removably securing said coverlay to said substrate element.

60. (Previously amended) The method of claim 41, wherein said introducing comprises substantially filling said slot formed through said tape and said at least one opening formed through said substrate element with said encapsulant material.

61. The method of claim 41, wherein said introducing comprises substantially encapsulating at least one intermediate conductive element electrically connecting said at least one bond pad to said at least one contact area.

62. (Previously amended) The method of claim 41, wherein said positioning said coverlay comprises forming said receptacle, including said slot and said at least one opening, within which said at least one bond pad is located.

63. (Amended) A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, said tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of said slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape with at least one opening formed through said substrate element being located at least partially over said slot; and

securing a coverlay to said substrate element to substantially seal said at least one opening, said coverlay and lateral edges of said at least one opening and said slot forming a receptacle.

64. (Previously amended) The method of claim 63, further comprising electrically connecting said at least one bond pad to at least one contact area located on a surface of said substrate element opposite said tape, proximate said at least one opening.

65. The method of claim 64, wherein said electrically connecting comprises connecting at least one intermediate conductive element between said at least one bond pad and said at least one contact area.

66. The method of claim 65, wherein said connecting said at least one intermediate conductive element comprises positioning said at least one intermediate conductive element at least partially within said slot and said at least one opening.

67. The method of claim 63, wherein said positioning said tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

68. The method of claim 67, wherein said positioning said substrate element comprises positioning over said tape a substrate element having a coefficient of thermal expansion similar to said coefficient of thermal expansion of the semiconductor die.

69. The method of claim 63, wherein said positioning said tape comprises positioning said tape with at least two regions of said slot extending laterally beyond said outer periphery of the semiconductor die.

70. The method of claim 63, further comprising securing said tape to the active surface of the semiconductor die.

71. The method of claim 70, wherein said securing comprises adhesively securing said tape to the active surface of the semiconductor die.

72. (Previously amended) The method of claim 64, wherein said positioning said substrate element comprises positioning over said tape a substrate element including a recessed area adjacent at least a portion of an edge of said at least one opening, said at least one contact area being located within said recessed area.

73. (Previously amended) The method of claim 63, wherein said positioning said substrate element comprises positioning over said tape a substrate element comprising at least one of an interposer and a carrier substrate.

74. (Previously amended) The method of claim 63, further comprising securing said substrate element to said tape.

75. (Previously amended) The method of claim 74, wherein said securing comprises adhesively securing said substrate element to said tape.

76. (Previously amended) The method of claim 63, wherein said positioning said coverlay comprises positioning over said substrate element a coverlay comprising a recess formed therein, said recess being positioned so as to communicate with said at least one opening formed through said substrate element when said positioning is effected.

78. (Twice amended) The method of claim 63, wherein said securing comprises adhesively securing said coverlay to said substrate element.

79. (Amended) The method of claim 63, wherein said securing comprises removably securing said coverlay to said substrate element.

Please add the following new claims:

-- 80. (New) A semiconductor device package, comprising:

a semiconductor die with a plurality of bond pads arranged on an active surface thereof;

a tape positioned over said active surface, said tape including at least one slot formed therethrough, each of said plurality of bond pads being exposed through said at least one slot, at least one end of said at least one slot extending beyond an outer periphery of said semiconductor die;

a substrate element positioned over said tape opposite said semiconductor die, said substrate element including a plurality of contact areas, each contact area of said plurality corresponding to a bond pad of said plurality of bond pads and electrically connected thereto by way of an intermediate conductive element that extends through at least one opening formed through said substrate element and aligned with said at least one slot of said tape, said substrate element further including a contact pad in communication with each contact area of said plurality of contact areas by way of a substantially laterally extending conductive trace;

a quantity of encapsulant material substantially filling a volume defined by said at least one slot of said tape and said at least one opening of said substrate element; and

a coverlay positioned over a surface of said substrate element opposite said tape, said coverlay substantially covering at least said at least one opening through said substrate element, contact pads of said substrate element being exposed through or beyond said coverlay.

81. The semiconductor device package of claim 80, wherein said plurality of bond pads is arranged substantially linearly along a central region of said active surface of said semiconductor die.

82. The semiconductor device package of claim 80, wherein said tape is formed from a material having a coefficient of thermal expansion similar to a coefficient of thermal expansion of a material of said semiconductor die.

83. The semiconductor device package of claim 82, wherein said substrate element has a coefficient of thermal expansion similar to said coefficient of thermal expansion of said material of said semiconductor die.

84. The semiconductor device package of claim 80, wherein both ends of said at least one slot formed through said tape extend beyond said outer periphery of said semiconductor die.

85. The semiconductor device package of claim 80, wherein said tape is adhesively secured to said active surface of said semiconductor die and to said substrate element.

86. The semiconductor device package of claim 80, wherein said substrate element comprises at least one of an interposer and a carrier substrate.

87. The semiconductor device package of claim 80, wherein said substrate element comprises silicon.

88. The semiconductor device package of claim 80, wherein said quantity of encapsulant material substantially encapsulates each intermediate conductive element.

89. The semiconductor device package of claim 88, wherein said quantity of encapsulant material protrudes above a major plane of an exposed surface of said substrate element opposite said semiconductor die.

90. The semiconductor device package of claim 80, wherein said substrate element includes a recessed area adjacent said at least one opening, each contact area of said plurality of contact areas being located within said recessed area.

91. The semiconductor device package of claim 90, wherein said quantity of encapsulant material substantially fills said recessed area.

92. The semiconductor device package of claim 91, wherein said quantity of encapsulant material substantially encapsulates each said intermediate conductive element.

93. The semiconductor device package of claim 91, wherein said quantity of encapsulant material does not extend substantially beyond a major plane of an exposed surface of said substrate element.

94. The semiconductor device package of claim 80, wherein said coverlay comprises a recessed area within which each intermediate conductive element is contained.

95. The semiconductor device package of claim 80, wherein said coverlay is secured to said surface of said substrate element.

96. The semiconductor device package of claim 95, wherein said coverlay is secured to said surface of said substrate element with an adhesive material.

97. The semiconductor device package of claim 96, wherein said adhesive material comprises a pressure sensitive adhesive material.

98. The semiconductor device package of claim 80, further comprising discrete conductive elements protruding from at least some of said contact pads.

99. A method for preparing a semiconductor die for packaging, comprising:

positioning a tape over at least an active surface of the semiconductor die, said tape including a slot through which at least one bond pad on the active surface of the semiconductor die is exposed, at least a portion of said slot extending laterally beyond an outer periphery of the semiconductor die;

positioning a substrate element over said tape with at least one opening formed through said substrate element being located at least partially over said slot; and

positioning a coverlay over said substrate element to substantially seal said at least one opening, said coverlay and lateral edges of said at least one opening and said slot forming a receptacle, contact pads exposed to a surface of said substrate element adjacent to which said coverlay is positioned being exposed through or beyond an outer periphery of said coverlay.

100. The method of claim 99, further comprising electrically connecting said at least one bond pad to at least one contact area located on a surface of said substrate element opposite said tape, proximate said at least one opening.

101. The method of claim 100, wherein said electrically connecting comprises connecting at least one intermediate conductive element between said at least one bond pad and said at least one contact area.

102. The method of claim 101, wherein said connecting said at least one intermediate conductive element comprises positioning said at least one intermediate conductive element at least partially within said slot and said at least one opening.

103. The method of claim 99, wherein said positioning said tape comprises positioning a tape having a coefficient of thermal expansion similar to a coefficient of thermal expansion of the semiconductor die.

104. The method of claim 103, wherein said positioning said substrate element comprises positioning over said tape a substrate element having a coefficient of thermal expansion similar to said coefficient of thermal expansion of the semiconductor die.

105. The method of claim 99, wherein said positioning said tape comprises positioning said tape with at least two regions of said slot extending laterally beyond said outer periphery of the semiconductor die.

106. The method of claim 99, further comprising securing said tape to the active surface of the semiconductor die.

107. The method of claim 106, wherein said securing comprises adhesively securing said tape to the active surface of the semiconductor die.

108. The method of claim 100, wherein said positioning said substrate element comprises positioning over said tape a substrate element including a recessed area adjacent at least a portion of an edge of said at least one opening, said at least one contact area being located within said recessed area.

109. The method of claim 99, wherein said positioning said substrate element comprises positioning over said tape a substrate element comprising at least one of an interposer and a carrier substrate.

110. The method of claim 99, further comprising securing said substrate element to said tape.

111. The method of claim 110, wherein said securing comprises adhesively securing said substrate element to said tape.

112. The method of claim 99, wherein said positioning said coverlay comprises positioning over said substrate element a coverlay comprising a recess formed therein, said recess being positioned so as to communicate with said at least one opening formed through said substrate element when said positioning is effected.

113. The method of claim 99, wherein said positioning said coverlay includes securing said coverlay to said substrate element.

114. The method of claim 113, wherein said securing comprises adhesively securing said coverlay to said substrate element.

115. The method of claim 113, wherein said securing comprises removably securing said coverlay to said substrate element.

116. The assembly of claim 21, wherein said coverlay is secured to said surface of said substrate element with an adhesive material.

117. The assembly of claim 116, wherein said adhesive material comprises a pressure sensitive adhesive material.

118. The assembly of claim 21, wherein said coverlay is removably secured to said surface of said substrate element.--